

AMENDMENTS TO THE CLAIMS

1 – 8 (Cancelled)

9. (Currently amended) A distributed multiprocessing system, comprising:
at least two hosts connected to a network, wherein each host of the distributed multiprocessing system has a processing unit and internal memory accessed by the processing unit; and,
a fault tolerant external memory unit, wherein each host further comprises an access device connected to the external memory unit through a memory bus which is connected with the internal memory [, and]] so that the access device provides the processing unit of the host with a transparent access to the external memory unit.
10. (Original) The system of claim 9, wherein the processing unit has an access time to the external memory unit less than three orders of magnitude larger than an access time to the internal memory.
11. (Previously presented) A distributed multiprocessing system comprising:
at least two hosts connected to a network, wherein each host has a processing unit and internal memory accessed by the processing unit; and
a fault tolerant external memory unit, wherein each host further comprises an access device connected to the external memory unit, and the access device provides the processing unit of the host with a transparent access to the external memory unit; and
wherein the processing unit has an access time to the external memory unit at least two orders of magnitude smaller than an access time to another host through the network.
12. (Original) The system of claim 9, wherein the access device in a host is connected to a bus, and access time to the external memory takes place in less than one cycle of the bus.

13. (Currently amended) ~~[[The]]~~ A distributed multiprocessing system of claim 9,
comprising:

at least two hosts connected to a network, wherein each host of the
distributed multiprocessing system has a processing unit and internal memory
accessed by the processing unit; and,

a fault tolerant external memory unit, wherein each host further comprises an
access device connected to the external memory unit, and the access device
provides the processing unit of the host with a transparent access to the external
memory unit,

wherein the access device has a memory-mapped connection to the
processing unit and a driver connected to both the memory-mapped connection and
the external memory unit.

14. (Currently amended) ~~[[The]]~~ A distributed multiprocessing system of claim 9,
comprising:

at least two hosts connected to a network, wherein each host of the
distributed multiprocessing system has a processing unit and internal memory
accessed by the processing unit; and,

a fault tolerant external memory unit, wherein each host further
comprises an access device connected to the external memory unit, and the access
device provides the processing unit of the host with a transparent access to the external
memory unit,

wherein the access device has an internal memory module-like
connection connected to the processing unit through a memory bus, and a driver
connected to both the internal memory module-like connection and the external memory
unit.

15. (Currently amended) ~~[[The]]~~ A distributed multiprocessing system of claim 9,
comprising:

at least two hosts connected to a network, wherein each host of the
distributed multiprocessing system has a processing unit and internal memory
accessed by the processing unit; and,

a fault tolerant external memory unit, wherein each host further comprises an access device connected to the external memory unit, and the access device provides the processing unit of the host with a transparent access to the external memory unit, wherein the external memory unit comprises:

at least two access server devices, each connected to the access device of a host; and,

a fault tolerant memory connected to each server device.

16. (Original) The system of claim 15, wherein the fault tolerant memory comprises a request server connected to the server devices.

17. (Original) The system of claim 16, further comprising:

two memory controllers connected to the request server, wherein each memory controller is connected to one or more memory banks.